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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,046	09/21/2000	Steven A. Lytle	LYTLE 18	8375

7590 07/31/2002

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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/667,046	Applicant(s) LYTLE, STEVEN A.	
	Examiner Hung K. Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,24,25,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,24,25,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant 's submission filed on 07/22/02 has been entered. An action on the RCE follows.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the device further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit, as recited in claim 25; the device further including a third dielectric layer located over the second dielectric layer and a landing pad located etween the second dielectric layer and the third dielectric layer, as recited in claim 27, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 21 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al. (PN 6,163,067).

Inohara et al. discloses, as shown in Figures 12-14, a semiconductor device comprising,

a first metal feature (25) located over a semiconductor surface and having a first etch stop layer (13a) and a first interlevel dielectric layer (13b) located thereover and a second etch stop layer (14a) and a second interlevel dielectric layer (14b) located over the first etch stop layer and the first interlevel dielectric layer;

an unsegmented via (32) located through the first and second etch stop layers and interlevel dielectric layers, the via extending to and contacting the first metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers; (Figure 21).

a second metal feature (16b) located adjacent the unsegmented via and extending through the second interlevel dielectric layers and the second etch stop layer and terminating at the first interleel dielectric layer;

a dual damascene structure adjacent the second metal feature and having a damascene trench portion (16) extending through the second interlevel dielectric layer and further including a damascene via portion (16c) extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

With regard to Claim 24, Inohara et al. discloses the via is a passing metal via with no passing metal feature.

With regard to Claim 25, Inohara et al. discloses the device further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inohara et al. (PN 6,163,067) in view of Huang et al. (PN 6,127,260, of record).

Inohara discloses, as shown in Figures 12-15, all of the claimed limitation except the device further including a third dielectric layer located over the second dielectric layer and a landing pad located between the second dielectric layer and the third dielectric layer, and a via that extends through the third dielectric layer and contacts the landing pad. However, Huang discloses a device having a third dielectric layer (45) located over a second dielectric layer (37) and a landing pad (42,43) located between the second dielectric layer and the third dielectric layer, and a via (47,48) that extends through the third dielectric layer and contacts the landing pad. Note Figure 10 of Huang et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Inohara further including a third dielectric layer located over the second dielectric layer and a landing pad located between the second dielectric layer and the third dielectric layer, and a via that extends through the third dielectric layer and contacts the landing pad, such as taught by Huang et al. in order to reduce the aspect ratio of the contact hole and to allow the via located in the third dielectric layer to be easily land on the landing pad.

5. Claims 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh (PN 6,225,207).

Parikh discloses, as shown in Figure 6B, a semiconductor device comprising,

a first feature (610) located over a semiconductor surface and having a first etch stop layer (611) and a first interlevel dielectric layer (612) located thereover and a second etch stop layer (614) and a second interlevel dielectric layer (616) located over the first etch stop layer and the first interlevel dielectric layer;

an unsegmented via (648) located through the first and second etch stop layers and interlevel dielectric layers, the via extending to and contacting the first feature, the via being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature (658) located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer;

a dual damascene structure adjacent the second metal feature and having a damascene trench portion (630) extending through the second interlevel dielectric layer and further including a damascene via portion (646) extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first feature.

Parikh discloses the first feature including structures and devices comprising interconnects. Note Col. 6, lines 63-66 of Parikh. Parikh does not disclose the first feature comprising metal. However, Parikh teaches to use the metal in the interconnects (dual damascene and via). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the interconnects of Parikh comprising metal because metal is commonly used for it is more conductivity and easier to form.

With regard to Claim 24, Inohara et al. discloses the via is a passing metal via with no passing metal feature.

6. Claims 25 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh (PN 6,225,207) in view of Huang et al. (PN 6,127,260, of record).

Parikh discloses, as shown in Figure 6D, all of the claimed limitations except the device further including transistors wherein the first feature is located over the transistors and interconnects the transistors. However, Huang et al. discloses a device includes a first metal feature (8) and transistors wherein the first metal feature is located over the transistors and interconnects the transistors. Note Figure 10 of Huang et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Parikh further including transistors wherein the first feature is located over the transistors and interconnects the transistors, such as taught by Huang et al. in order to form a desire operative integrated circuit.

With regard to Claims 27 and 28, Inohara discloses all of the claimed limitation except the device further including a third dielectric layer located over the second dielectric layer and a landing pad located between the second dielectric layer and the third dielectric layer, and a via that extends through the third dielectric layer and contacts the landing pad. However, Huang discloses a device having a third dielectric layer (45) located over a second dielectric layer (37) and a landing pad (42,43) located between the second dielectric layer and the third dielectric layer, and a via (47,48) that extends through the third dielectric layer and contacts the landing pad. Note Figure 10 of Huang et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Parikh further including a third dielectric layer located over the second dielectric layer and a landing pad located between the second dielectric layer and the third dielectric layer, and a via that extends through the third dielectric layer and contacts the landing pad, such as taught by Huang et al. in order to reduce the

aspect ratio of the contact hole and to allow the via located in the third dielectric layer to be easily land on the landing pad.

Response to Arguments

7. Applicant's arguments with respect to claim 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-5:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

July 29, 2002

Steven Loke
Primary Examiner

Steven Loke